## **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurais	Time Stamp
L1	2	"6034832".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/03 22:58
L2	2	"5832173".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:21
L3	1	"5832173".pn. and (start\$3 and end\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:05
L4	2	"5832173".pn. and (mark\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:31
L5	0	"5134499".pn. and (bit or byte)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:16
L6	0	"5134499".pn. and (rate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:16
L7	0	"5832173".pn. and (bit or byte or rate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:21
L8	0	"5134499".pn. and (bit or byte or rate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:24

## **EAST Search History**

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L9	2	"5134499".pn. and (position)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:24
L10	0	"5134499".pn. and (stripe)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:27
L11	1	"5134499".pn. and (position with (shown or display))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:28
L12	1	"5832173".pn. and (mark\$3 with speed)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:33
L13	0	"5832173".pn. and (mark\$3 with image)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:33
L14	0	"5832173".pn. and (mark\$3 with program)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:34
L15		"5832173".pn. and (mark\$3 same program)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:34
L16	0	"5832173".pn. and (mark\$3 same genre)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/04 00:34

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passivation layer above the metal pad, for connection of a bonding wire to the metal pad.

Claim 7 (currently amended): The method of claim 5, wherein the metal guard ring has an inside edge and an outside edge[[,]] the slot is narrower than the metal guard ring, and the inside edge and the outside edge of the metal guard ring are covered by the passivation layer.

Claim 8 (currently amended): The method of claim 7, wherein:

the semiconductor chip has a corner; and

the metal guard ring has a slit in the metal guard ring is disposed between said inside edge and said outside edge at least at said corner[[;]] and the slot in the passivation layer avoids said slit, leaving said slit covered by the passivation layer.

Claim 9 (currently amended): The method of claim 7 [[8]], wherein the slot in the passivation layer is disposed between [[said]] the slit and the outside edge of the metal guard ring.

